IN THE CLAIMS

Please amend the Claims as follows:

1-40. (Canceled)

41. (original) A stitched MONOS memory array comprising:

three resistive layers wherein said three resistive layers are vertically stacked as a bottom, middle, and top resistive layer and wherein said bottom and middle resistive layers run in parallel to each other and wherein said top resistive layer runs orthogonally to said bottom and middle resistive layers; and

stitches periodically contacting each of said resistive layers to a respective upper conductive layer wherein said stitches comprise:

connections from said middle resistive layer to a bottom conductive layer overlying said top resistive layer;

contact/via stacks from said bottom resistive layer to a top conductive layer;

a middle conductive layer connecting cut ends of said middle resistive layer wherein said middle conductive layer overlies said bottom conductive layer and underlies said top conductive layer and wherein said middle conductive layer loops around said contact/via stacks; and

connections from said top resistive layer to said middle conductive layer.

42. (original) The memory array according to Claim 41 wherein said stitches are located on alternate sets of resistive lines.

43. (original) The memory array according to Claim 41 wherein said bottom and middle resistive lines are a bit line and a control gate line and wherein said top resistive line is a word gate line.

44. (original) The memory array according to Claim 41 wherein said bottom and middle resistive lines are a word line and a control gate line and wherein said top resistive line is a bit line.

45. (original) The memory array according to Claim 41 wherein said stitches reduce resistance of said MONOS memory array.

46. (original) The memory array according to Claim 41 wherein said stitches lie within a cell size limited by a minimum metal pitch.

47. (original) A stitched MONOS memory array comprising:

three resistive layers wherein said three resistive layers are vertically stacked as a bottom, middle, and top resistive layer and wherein said bottom and middle resistive layers run in parallel to each other and wherein said top resistive layer runs orthogonally to said bottom and middle resistive layers; and

stitches periodically contacting each of said resistive layers by a respective upper conductive layer wherein said stitches comprise:

connections from said top resistive layer to a bottom conductive layer overlying said top resistive layer;

contact/via stacks from said bottom resistive layer to a top conductive layer;

a bottom conductive layer connecting cut ends of said middle resistive layer wherein said bottom conductive layer loops around said contact/via stacks; and

connections from said middle resistive layer to a middle conductive layer wherein said middle conductive layer overlies said bottom conductive layer and underlies said top conductive layer.

48. (original) The memory array according to Claim 47 wherein said stitches lie on alternate sets of resistive lines.

49. (original) The memory array according to Claim 47 wherein said bottom and middle resistive lines are a bit line and a control gate line and wherein said top resistive line is a word gate line.

50. (original) The memory array according to Claim 47 wherein said bottom and middle resistive lines are a word line and a control gate line and wherein said top resistive line is a bit line.

51. (original) The memory array according to Claim 47 wherein said stitches reduce resistance of said MONOS memory array.

52. (original) The memory array according to Claim 47 wherein said stitches lie within a cell size limited by a minimum metal pitch.

53. (currently amended) A stitched MONOS memory array comprising:

a plurality of memory cells in a MONOS memory array wherein each memory cell comprises:

a storage cell on either side of a word gate;

a ~~bit~~ diffusion junction underlying each of said storage cells wherein each of said ~~bit~~ diffusions ~~junctions~~ is shared with an adjacent storage cell of an adjacent memory cell; and

a control gate overlying each of said storage cells electrically isolated from underlying said ~~bit~~ diffusion junctions wherein said control gates and said ~~bit~~ diffusions ~~junctions~~ run in parallel and wherein said word gates run orthogonally to said control gates and said ~~bit~~ diffusions ~~junctions~~;

wherein word gates in said array form word lines, said control gates in said array form control gate lines, and said ~~bit~~ diffusions ~~junctions~~ in said array form bit lines;

connections from said control gate lines to a bottom conductive layer overlying said word gate lines;

contact/via stacks from said bit lines to a top conductive layer;

a middle conductive layer connecting cut ends of said control gate lines wherein said middle conductive layer overlies said bottom conductive layer and underlies said top conductive layer and wherein said middle conductive layer loops around said contact/via stacks; and

connections from said word gate lines to said middle conductive layer.

54. (original) The memory array according to Claim 53 wherein said connections lie on alternate sets of control gate lines, bit lines, and word lines.

55. (currently amended) A stitched MONOS memory array comprising:

a plurality of memory cells in a MONOS memory array wherein each memory cell comprises:

a storage cell on either side of a word gate;

a ~~bit~~ diffusion junction underlying each of said storage cells wherein each of ~~bit~~ diffusions ~~junctions~~ is shared with an adjacent storage cell of an adjacent memory cell; and

a control gate overlying each of said storage cells electrically isolated from underlying said ~~bit~~ diffusion junctions wherein said control gates and said ~~bit~~ diffusions ~~junctions~~ run in parallel and wherein said word gates run orthogonally to said control gates and said ~~bit~~ diffusions ~~junctions~~;

wherein word gates in said array from word lines, said control gates in said array form control gate lines, and said ~~bit~~ diffusions ~~junctions~~ in said array form bit lines;

connections from said control gate lines to a middle conductive layer overlying said word gate lines;

contact/via stacks from said bit lines to a top conductive layer wherein said top conductive layer overlies said middle conductive layer;

a bottom conductive layer connecting cut ends of said control gate lines wherein said bottom conductive layer underlies said middle conductive layer and wherein said bottom conductive layer loops around said contact/via stacks; and

connections from said word gate lines to said bottom conductive layer.

56. (original) The memory array according to Claim 55 wherein said connections lie on alternate sets of control gate lines and bit lines.

57. (currently amended) A stitched MONOS memory array comprising:

a plurality of memory cells in a MONOS memory array wherein each memory cell comprises:

a storage cell on either side of a word gate;

a ~~bit~~ diffusion junction underlying each of said storage cells wherein each of ~~bit~~ diffusions ~~junctions~~ is shared with an adjacent storage cell of an adjacent memory cell; and

a control gate overlying each of said storage cells electrically isolated from underlying said ~~bit~~ diffusion junctions wherein said control gates and said ~~bit~~ diffusions ~~junctions~~ run in parallel and wherein said word gates run orthogonally to said control gates and said ~~bit~~ diffusions ~~junctions~~;

wherein word gates in said array from word lines, said control gates in said array form control gate lines, and said ~~bit~~ diffusions ~~junctions~~ in said array form bit lines;

stitches periodically contacting each of said word lines, control gate lines, and bit lines by a respective upper conductive layer wherein said contacting comprises:

connections from said control gate lines to a middle conductive layer overlying said word gate lines;

contact/via stacks from said bit lines to a top conductive layer wherein said top conductive layer overlies said middle conductive layer;

a bottom conductive layer connecting cut ends of said control gate lines wherein said bottom conductive layer underlies said middle conductive layer and wherein said bottom conductive layer loops around said contact/via stacks; and

connections from said word gate lines to said bottom conductive layer; and

select transistors in areas of said stitching between sub-arrays of said MONOS memory cells.

58. (original) The memory array according to Claim 57 wherein said stitches lie on alternate sets of control gate lines and bit lines.

59. (original) The memory array according to Claim 57 wherein said select transistors comprise:

extensions of alternate said bit diffusions past an edge of said control gates;

bit line select transistors placed alternately with said extended bit diffusions on either side of each of said sub-arrays and horizontally across said extended bit diffusions wherein unextended said bit diffusions are connected to said bit lines by contact stacks to said middle conductive layer.

60. (original) The memory array according to Claim 57 wherein said select transistors comprise:

pairs of control gate select transistors between said sub-arrays; and

control gate contacts over shallow trench isolation areas wherein center control gate contacts lie between two control gate select transistors of a pair and wherein outer control gate contacts lie on outer sides of each of said pairs, wherein said center control gate contacts are connected to said control gate lines by said top conductive layer and wherein said outer control gates contact control gates of a nearest said sub-array.

61. (original) The memory array according to Claim 60 wherein each of said sub-array control gates is connected by said bottom conductive layer to a source diffusion of said control gate select transistor.

62. (original) The memory array according to Claim 60 wherein each of said sub-array control gates is extended to a source diffusion of a corresponding said control gate select transistor thereby directly connecting each of said control gates to a corresponding control gate select transistor source diffusion.

63. (original) The memory array according to Claim 60 wherein said control gate select transistors are chosen from the group consisting of: an N-channel device in an isolated P-well, and a P-channel device in an independent N-well.

64. (original) The memory array according to Claim 60 wherein said pairs of control gate select transistors run in parallel with said word lines and perpendicular to said bit lines and said control gate lines.

65. (original) The memory array according to Claim 57 wherein said select transistors comprise:

extensions of alternate said bit diffusions past an edge of said control gates;

bit line select transistors placed alternately with said extended bit diffusions on either side of each of said sub-arrays and horizontally across said extended bit diffusions wherein unextended said bit diffusions are connected to said bit lines by contact stacks to said middle conductive layer;

pairs of control gate select transistors placed out of phase with and between two of said bit line select transistors inside two edges of two said sub-arrays; and

control gate contacts over shallow trench isolation areas wherein center control gate contacts lie between two control gate select transistors of a pair and wherein outer control gate contacts lie on outer sides of each of said pairs, wherein said center control gate contacts are connected to said control gate lines by said top conductive layer and wherein said outer control gates contact control gates of a nearest said sub-array.

66. (original) The memory array according to Claim 65 wherein each of said sub-array control gates is connected by said bottom conductive layer to a source diffusion of said control gate select transistor.

67. (original) The memory array according to Claim 65 wherein each of said sub-array control gates is extended to a source diffusion of a corresponding said control gate select transistor thereby directly connecting each of said control gates to a corresponding control gate select transistor source diffusion.

68. (original) The memory array according to Claim 65 wherein said control gate select transistors are chosen from the group consisting of: an N-channel device in an isolated P-well, and a P-channel device in an independent N-well.

69. (original) The memory array according to Claim 65 wherein said pairs of control gate select transistors run in parallel with said word lines and perpendicular to said bit lines and said control gate lines.

70. (currently amended) A stitched MONOS memory array comprising:

a plurality of memory cells in a MONOS memory array wherein each memory cell comprises:

a storage cell on either side of a word gate;

a ~~bit~~ diffusion junction underlying each of said storage cells wherein each of said ~~bit~~ diffusion<u>s</u> ~~junctions~~ is shared with an adjacent storage cell of an adjacent memory cell; and

a control gate overlying each of said storage cells electrically isolated from underlying said ~~bit~~ diffusion junctions wherein said control gates and said word gates run in parallel and wherein said ~~bit~~ diffusion<u>s</u> ~~junctions~~ run orthogonally to said control gates and said word gates;

wherein word gates in said array form word lines, said control gates in said array form control gate lines, and said ~~bit~~ diffusions ~~junctions~~ in said array form bit lines;

connections from said bit lines to a bottom conductive layer overlying said word gate lines;

connections from said control gate lines to a middle conductive layer;

contact/via stacks from said word gate lines to a top conductive layer overlying said middle conductive layer; and

a bottom conductive layer contacting said control gate lines wherein said bottom conductive layer underlies said middle conductive layer and loops around said contact/via stacks.

71. (original) The memory array according to Claim 70 wherein said connections lie on alternate sets of control gate lines and word lines.

72. (original) The memory array according to Claim 70 wherein said middle conductive line and said top conductive line are shifted by half a metal pitch, wherein said middle conductive layer also loops around said contact/via stack, and wherein said connections lie on every control gate line and on alternate sets of word lines.